SOI SEMICONDUCTOR CONFIGURATION

AND METHOD OF FABRICATING THE SAME

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Background of the Invention:

Field of the Invention:

The invention lies in the field of semiconductor manufacture. Specifically, the invention relates to a SOI semiconductor

10 configuration, i.e., a structure formed with a base layer (e.g. substrate) of semiconductor material, an insulation layer on the base layer, and a layer of monocrystalline silicon disposed on and adjoining the insulation layer. The invention also pertains to a method of manufacturing the SOI

15 structure.

It has been known in the pertinent art to construct MOS field-effect transistors (MOSFETs) on silicon-on-insulator (SOI) substrates. A significant advantage of the technology is that,

20 in comparison with conventional MOSFETs constructed on silicon substrates, it is possible to achieve complete electrical depletion of the channel during operation. The consequence of this is that very low operating voltages (below 1 V) can be achieved, which, in turn, makes it possible to realize "low-

25 power" CMOS applications with low power consumption. A further beneficial aspect of SOI technology is that very high packing

densities can be realized on account of the dual -- lateral
and vertical -- insulation effect of the buried oxide layer.
An up-to-date overview over SOI technology and its possible
applications in the future is provided in the article

5 "Silicon-on-Insulator-Technologie: Neue 'Low Power'-CMOS
Anwendungen mit Betriebsspannungen kleiner 0.9 V" [Silicon-on-
Insulator Technology: New 'Low Power' CMOS Applications with
Operating Voltages of Less than 0.9 V], Pindl and Risch, Phys.
Bl. 54 (1998), No. 4.

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It is known in the art that, in conventional MOSFETs
constructed on Si substrates, "hot charge carriers" can cause
damage to the gate oxide. The "hot charge carriers" thereby
rupture Si-H bonds in the interface between the channel

15 silicon and the gate oxide and produce interface states
(traps) which are undesirable because they lead to a change in
various transistor parameters. The usual procedure for
avoiding this so-called HC degradation (HC = hot carrier) is
to provide a gentle transition in the drain doping. This

20 measure, known as LDD doping (LDD = Lightly Doped Drain),
reduces the production of hot charge carriers and hence damage
to the gate oxide. It is disadvantageous, however, that the
transistor properties can be adversely influenced by the LDD
doping.

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Summary of the Invention:

It is accordingly an object of the invention to provide a semiconductor configuration based on SOI technology, which overcomes the above-mentioned disadvantages of the heretofore-

5 known devices and methods of this general type and which makes it possible to form high-performance SOI transistors on it or which already comprises such high-performance SOI transistors. It is a further object of the invention to specify a method for fabricating such a semiconductor configuration.

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With the foregoing and other objects in view there is provided, in accordance with the invention, a semiconductor configuration, comprising:

a base layer made of semiconductor material, in particular a
15 substrate;

an insulation layer arranged above the base layer;

a monocrystalline silicon layer disposed above and adjoining the insulation layer, the monocrystalline silicon layer and the insulation layer forming an interface therebetween; and

20 a passivating substance X forming Si-X bonds at the interface between the insulation layer and the monocrystalline silicon layer, whereby a bond energy of one of the Si-X bonds is greater than a bond energy of an Si-H bond.

The semiconductor configuration according to the invention is thus comparable, in terms of its construction, with a conventional SOI substrate, except for the passivating

5   substance X that is incorporated, with the formation of Si-X bonds, in the region of the interface between the insulation layer and the monocrystalline silicon layer above the latter. Since the Si-X bonds have a greater bond energy than Si-H bonds, it is considerably more difficult for hot charge

10   carriers to rupture them. Therefore, the Si-X bonds remain intact even in the event of comparatively high kinetic charge carrier energies, as a result of which the production of undesirable interface states in the transition region between the insulation layer and the monocrystalline silicon layer is

15   distinctly reduced.

If SOI transistors are formed in the semiconductor configuration according to the invention by means of process steps that will subsequently be described in more detail, the

20   consequence of the incorporation of passivating substance in accordance with the invention is that damage to the SOI insulation layer by hot charge carriers and associated impairment of transistor properties cannot occur, or can occur only to a very small extent.

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In accordance with an added feature of the invention, the passivating substance X is a halogen or nitrogen. The halogens, in particular fluorine and chlorine, and also nitrogen form a bond with silicon whose bond energy is

5   distinctly higher than the bond energy of the Si-H bond.

In accordance with an additional feature of the invention, there are provided:

a plurality of laterally adjacent, differently doped regions formed in the monocrystalline silicon layer, the regions forming a source region, a channel region, and a drain region of a MOSFET; and

a gate oxide layer disposed above the channel region and an electrical connection structure forming a gate of the MOSFET disposed on the gate oxide layer.

In this case, the insulation layer creates insulation - which is resistant to HC degradation - of the source, channel and drain region of the SOI MOSFET with respect to the base layer

20 and thus ensures a high transistor drain current.

In accordance with another feature of the invention, the channel region in the monocrystalline silicon layer and the gate oxide layer form an interface therebetween, and the

passivating substance X is also present at the interface between the channel region and the gate oxide layer, with a formation of Si-X bonds. Not only the insulation layer but also the gate oxide layer is then passivated, i.e. protected

5 from HC degradation. The concentration of the passivating substance X at the interfaces may be approximately 10^{18} cm^{-3} in this case.

In accordance with a further feature of the invention, the

10 semiconductor configuration comprises a plurality of mutually adjacent MOSFETs which isolated from one another by Mesa insulation. The electrical insulation of adjacent MOSFETs can, in principle, be effected by any one of the known technologies, for example LOCOS (Local Oxidation of Silicon)

15 or STI (Shallow Trench Isolation). It is preferable, however, for adjacent MOSFETs to be electrically isolated from one another by Mesa insulation. In this technology, the silicon layer in the region between two SOI MOSFETs is removed down to the underlying insulation layer, in which case high packing

20 densities can advantageously be obtained.

With the above and other objects in view there is also provided, in accordance with the invention, a method of fabricating the semiconductor configuration. The method

25 comprises the following steps:

providing a semiconductor structure having the base layer, the insulation layer, and the monocrystalline silicon layer;

introducing the passivating substance X into one of the insulation layer and the monocrystalline silicon layer during

5 or after the fabrication of the semiconductor structure; and

heat-treating the semiconductor structure with the passivating substance X.

In other words, the passivating substance X can be introduced

10 into the insulation layer and/or the monocrystalline silicon layer either during or after the fabrication of the semiconductor structure. The subsequent heat treatment causes the passivating substance X thus introduced to diffuse into the region of the interface, where it replaces existing Si-H

15 bonds with Si-X bonds.

In accordance with a preferred mode of the invention, the passivating substance X is introduced by ion-implantation into the corresponding layer(s). The ion implantation technique

20 enables the passivating substance X to be deposited in a manner allowing a highly targeted dose and with positional accuracy. Furthermore, it is advantageous that the passivating substance X can be introduced into the insulation layer through the upper monocrystalline silicon layer or else, if

appropriate, further covering layers as well. Therefore, the introduction of the passivating substance X can chronologically succeed the fabrication of the SOI semiconductor structure, with the result that commercially

5   available prefabricated SOI semiconductor structures can also be used as a basis for the method according to the invention.

The use of an implantation step for introducing the passivating substance X into an SOI semiconductor structure

10   may be advantageous particularly when the SOI semiconductor structure is also fabricated by means of an ion implantation process. This is the case with the so-called SIMOX (Separation by Implementation of Oxygen) technology, in which the insulation layer is formed in the form of a buried SiO_2 layer

15   by implantation of a high oxygen dose into a monocrystalline silicon substrate. The implantation step for introducing the passivating substance X can then directly follow the oxygen implantation step for forming the SOI semiconductor structure, and, in a manner which is beneficial in terms of fabrication

20   engineering, the two steps can be carried out in one and the same implantation installation. Furthermore, it is also possible to perform the passivating substance implantation step according to the invention prior to the oxygen implantation.

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A further possibility is to introduce the passivating
substance X into the SOI semiconductor structure by means of a
diffusion step. A suitable fabrication method for this
purpose, for SOI semiconductor structures, is known in the art
5   as a BESOI (Bonded Etched-back Silicon on Insulator) method.
In this method, two silicon semiconductor substrates are
firstly provided in each case with a surface oxide layer. The
two silicon semiconductor substrates are then joined by
contact-connection of their oxide layers and one of the
10   silicon semiconductor substrates is removed, except for a thin
residual layer, for the purpose of forming the upper
monocrystalline silicon layer. In accordance with a design
variant according to the invention, the BESOI method is now
modified such that the passivating substance X is introduced
15   into one or both oxide layers before the joining of the two
silicon semiconductor substrates and/or into one of the
silicon semiconductor substrates before or after the oxidation
step. In this case, the introduction of the passivating
substance X can be performed simply by thermal doping
20   (diffusion of the passivating substance from a passivating
substance gas into the corresponding layer), since the layers
to be passivated are uncovered before the joining of the two
silicon semiconductor substrates.

25   In order to obtain short diffusion paths in the heat-treatment
step which is to be carried out after the introduction of the

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passivating substance X, it is expedient for the implantation maximum of the passivating substance X to be placed in the vicinity of the interface with the monocrystalline silicon layer.

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A covering oxide layer is preferably applied on the top monocrystalline silicon layer. The covering oxide layer may serve as a screen layer in subsequent implantation steps.

10 The introduction of the passivating substance X into the insulation layer and/or the monocrystalline silicon layer can be performed either before or after any patterning of the monocrystalline silicon layer that is to be carried out. One advantage of the last-mentioned possibility is that the

15 passivating substance X, when being introduced into the insulation layer and/or the silicon layer, can simultaneously be incorporated into so-called spacers which have been formed beforehand on steps of the patterned monocrystalline silicon layer. In this way, the spacers are passivated as well, as a

20 result of which the formation of undesirable Mesa sidewall transistors can be effectively suppressed.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

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Although the invention is illustrated and described herein as embodied in an SOI semiconductor configuration and method for fabricating the same, it is nevertheless not intended to be limited to the details shown, since various modifications and

5   structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention,

10   however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

15   Brief Description of the Drawings:

Figs. 1a to 1f are diagrammatic vertical sectional views of a sequence with a first design variant, in which the passivating substance X is introduced prior to the patterning of the silicon layer by implantation into a buried oxide layer;

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Figs. 2a to 2f are diagrammatic vertical sectional views of a sequence with a second design variant, in which the passivating substance X is introduced prior to the patterning of the silicon layer by implantation into the silicon layer;

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Figs. 3a to 3f are diagrammatic vertical sectional views of a
sequence with a third design variant of the invention, in
which the passivating substance X is introduced after the
patterning of the silicon layer by implantation into a buried
5   oxide layer; and

Figs. 4a to 4f are diagrammatic vertical sectional views of a
sequence with a fourth design variant of the invention, in
which the passivating substance X is introduced after the
10   patterning of the silicon layer by implantation into the
silicon layer.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and
15   first, particularly, to Figs. 1a to 1f thereof, there is seen
an SOI semiconductor structure 5 that comprises an Si base
layer 1, which is formed by an Si substrate and is adjoined by
a buried oxide layer 2, on which a monocrystalline silicon
layer 3 is overlaid. By way of example, the SOI semiconductor
20   structure 5 may be fabricated according to the SIMOX or BESOI
technologies and is commercially available as a finished
product. Furthermore, the Si base layer 1 and the
monocrystalline silicon layer 3 may already be p- or n-
predoped by the manufacturer.

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With reference to Fig. 1a, a screen oxide layer 4 is first

formed on the SOI semiconductor structure 5. The screen oxide

layer 4 may be formed for example by thermal oxidation of the

monocrystalline silicon layer 3 or by deposition of a TEOS

5   (tetraethylorthosilicate) layer by means of a CVD process.

With reference to Fig. 1b, the passivating substance X is

subsequently incorporated in a whole-area or large-area

application by implantation into the buried oxide layer 2. The

10   implantation step is illustrated by arrows 6. By way of

example, nitrogen, fluorine or chlorine is used as the

passivating substance X. The incorporation process can be

controlled in a highly targeted manner with regard to the

incorporation depth, the incorporation dose and the

15   incorporation profile. Since the passivating substance X is

intended to be employed in the region of the interface 7

between the monocrystalline silicon layer 3 and the buried

oxide layer 2, conditions which cause the implantation maximum

8 to lie a short way underneath the interface 7 are chosen in

20   the implantation step.

A heat-treatment step is subsequently carried out. In the

process, the passivating substance X implanted into the buried

oxide layer 2 diffuses to the interface 7, the passivating

25   substance distribution 8' also being shifted into the region

of the interface 7. In the process, Si-H bonds present in the

region of the interface 7 are replaced by the more energy-stable Si-X bonds. As a result, the damage resistance of the buried oxide layer 2 with respect to HC degradation is increased in the manner already described. Furthermore, the

5 heat-treatment step effects annealing of damage or defects which have occurred during the implantation step in the upper layers 3 and 4. Fig. 1c illustrates the situation after the heat-treatment step has been carried out. The concentration of the passivating substance X may be approximately 10^{18} cm^{-3}, for

10 example.

Figs 1d to 1f show, by way of example, further process steps which are carried out for the patterning and insulation of the monocrystalline silicon layer 3 for the purpose of forming an

15 SOI MOSFET. Such steps are also necessary to construct an integrated CMOS circuit on the SOI semiconductor structure 5. First of all, in accordance with Fig. 1d, the screen oxide layer 4 and the monocrystalline silicon layer 3 are removed, except for locally residual layer regions 3', 4', using

20 customary photolithographic masking techniques and etching steps. As a result, the monocrystalline layer region 3' is electrically insulated from corresponding, adjacent layer regions (not illustrated in Fig. 1d). The method shown here is known as Mesa insulation in the art. Other insulation methods

25 (for example LOCOS, STI) can also be employed instead of Mesa insulation.

According to Fig. 1e, the peripheral walls of the layer
regions 3', 4' are covered with spacers 9.·The spacers 9 serve
to additionally insulate the peripheral walls of the free-
5   standing layer regions 3', 4'.

Finally, according to Fig. 1f, the channel doping of the SOI
MOSFET to be produced is brought about by a further
implantation step. The channel implantation step is indicated
10   by the arrows 10.

The implantation steps (Fig. 1b, Fig. 1f) can be carried out
in a positionally selective manner by using non-illustrated
implantation masks. In particular, the passivating substance X
15   can be implanted in a targeted manner for example only into n-
channel transistors.

The second method variant illustrated in Figs 2a to 2f differs
from the first method variant shown in Figs 1a to 1f
20   essentially merely in the fact that the implantation maximum 8
lies in the monocrystalline silicon layer 3 rather than in the
buried oxide layer 2. In this case, the implanted dose of the
passivating substance X should lie below the amorphizing dose
in silicon. According to Fig. 2c, in this variant the
25   implanted passivating substance X diffuses both to the
interface 7 between buried oxide layer 2 and monocrystalline

silicon layer 3 and to an interface 11 between monocrystalline silicon layer 3 and screen oxide layer 4. As a result, after removal of the screen oxide layer 4 and subsequent growth of a gate oxide layer on the monocrystalline silicon layer 3, the

5   latter still contains sufficient passivating substance X in the region near the interface to increase the resistance of the gate oxide layer as well with respect to damage caused by hot charge carriers.

10   The steps of patterning/insulation, spacer formation and channel implantation as illustrated in Figs 2d to 2f are carried out analogously to the steps illustrated in Figs 1d to 1f.

15   The heat-treatment step shown in Fig. 2c may also be carried out after the Mesa insulation (Fig. 2d) and the provision of the spacers 9 (Fig. 2e). In that case, the passivating substance X is situated only in those portions of the interfaces 7, 11 which are covered by the layer regions 3',

20   4', i.e. in the active regions. When spacers 9 made of silicon oxide and a nitrogen passivating substance X are used, the spacer inner walls adjoining the peripheral walls of the layer regions 3', 4' are also nitrided in this case. During the subsequent channel doping (Fig. 2f) this inhibits the

25   outdiffusion of channel dopant into the spacers and

consequently suppresses the formation of Mesa sidewall
transistors in a desired manner.

Halogens used as passivating substance X, on the other hand,

5   accelerate the diffusion of channel dopant, in particular

boron, into spacers 9 formed from silicon oxide. In order to

avoid sidewall transistors, Mesa spacers 9 formed from silicon

nitride are used in this case.

10   In the case of the third design variant of the method

according to the invention as illustrated in Figs 3a to 3f,

the passivating substance X is introduced into the buried

oxide layer 2 as in the case of the first design variant (Figs

1a to f). The corresponding implantation step is illustrated

15   in Fig. 3d. In contrast to the first design variant, however,

the patterning/insulation and also the formation of the Mesa

spacers 9 and subsequent thermal oxidation of the

monocrystalline layer region 3' for the purpose of forming the

screen layer region 4' (see Figs. 3a to 3c) eventually take

20   place prior to the passivating substance implantation step in

this case.

If the spacers 9 are composed of silicon oxide, the

consequence of this is that the passivating substance X is

25   also implanted into the Mesa spacers 9, since the implantation

depth is smaller in silicon oxide than in monocrystalline

silicon. As a result, the suppressing – which was described in the case of the second design variant – of Mesa sidewall transistors in the event of using nitrogen as passivating substance X takes place in this case as well. Fig. 3e shows

5   the nitrogen distribution 8' resulting after the heat-treatment step in the region of the interface 7 and at the peripheral walls of the monocrystalline layer region 3'. In the event of using halogens as passivating substance, spacers 9 composed of silicon nitride should be used – as already

10   described in connection with the second design variant.

Fig. 3f again shows the channel implantation step.

If the heat-treatment step illustrated in Fig. 3e is not
15   carried out until after the channel implantation (Fig. 3f), the well photomask (not illustrated) used for the channel implantation can be used to mask the implantation of the passivating substance X as well, with no additional outlay. In this procedure, too, the passivating substance X is implanted

20   into the Mesa spacers 9, provided that the latter are composed of silicon oxide.

Figs 4a to 4f show a fourth design variant of the method according to the invention. In this case, as in the case of
25   the third design variant, the patterning/insulation, the Mesa spacer formation and the thermal oxidation of the active

silicon layer region 3' (Figs 4a to 4c) take place before the introduction of the passivating substance X by an implantation step (Fig. 4d). In contrast to the third design variant, a lower implantation energy is chosen in this case, with the

5   result that the implantation maximum 8 lies within the monocrystalline Si layer region 3'. Implantation into the spacers 9 takes place in this case as well. Fig. 4e shows the distribution 8' of the passivating substance X after the heat-treatment step. The advantage of this design variant resides

10   in the additional passivation (halogenation or nitriding) of the gate oxide to be grown on later (cf. the second design variant as well) and – given the use of nitrogen implantation and oxide spacers 9 – in the nitriding of the Mesa spacer inner side for the purpose of suppressing Mesa sidewall

15   transistors. Fig. 4e shows that the active monocrystalline silicon layer region 3' is completely passivated on all sides.

If halogens are used as the passivating substance X, spacers 9 made of silicon nitride should again be used. In addition, as

20   in the case of the third design variant, it is possible, during the masking of the passivating substance implantation step (Fig. 4d), to use the same mask as for the channel implantation step (Fig. 4f).

25   The table below shows the bond energies of silicon with hydrogen and also the passivating substances nitrogen,

fluorine and chlorine. It is evident that the Si-X bond has a distinctly higher bond energy when the above-mentioned passivating substances X are used than when hydrogen is used as the bonding partner.

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Table: Bond energies of silicon bonds

Bond	Bond Energy [eV]
Si-H	3.1
Si-N	4.6
Si-F	5.7
Si-Cl	4.7